

EXHIBIT 038

U.S. Patent No. 7,366,818 (Radulescu & Goossens)

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	OnePlus Product Including Snapdragon System on Chip ¹
<p>1. Integrated circuit comprising a plurality of processing modules (M, S) said modules being disposed on the same chip, and</p>	<p>Without conceding that the preamble of claim 1 of the '818 Patent is limiting, the OnePlus 10T (hereinafter, the “OnePlus product”) includes an integrated circuit.</p> <p>For example, the OnePlus product includes the Snapdragon 8+ Gen 1 Mobile Platform system on chip (hereinafter, the “Snapdragon SoC”).</p> <div data-bbox="501 548 991 1081">  </div> <div data-bbox="1115 634 1472 690"> <h2>OnePlus 10T</h2> </div> <div data-bbox="1115 717 1745 748"> <p>Powered by Snapdragon 8+ Gen 1 Mobile Platform</p> </div> <div data-bbox="1115 776 1885 1002"> <p>OnePlus 10T 5G is the speed-leading flagship delivering ultimate performance. Driven relentlessly by the fastest charging in OnePlus history and the powerful Snapdragon 8+ Gen 1 mobile platform, this is a phone built to evolve beyond speed. It has Qualcomm FastConnect 6900 for premium Wi-Fi connectivity and a Kryo CPU for unbeatable performance.</p> </div> <div data-bbox="495 1083 1711 1120"> <p>https://www.qualcomm.com/snapdragon/device-finder/smartphones/oneplus-10t</p> </div>

¹ The OnePlus product is charted as a representative product made used, sold, offered for sale, and/or imported by OnePlus. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein

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	<p>The Snapdragon SoC comprises a plurality of processing modules, for example Qualcomm Adreno GPU; Qualcomm Kryo CPU; Qualcomm Hexagon Processor; and Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU):</p> <div data-bbox="514 414 934 552">  <p>Snapdragon 8+ mobile platform Gen 1</p> </div> <div data-bbox="1528 438 1827 462">SPECIFICATIONS & FEATURES</div> <div data-bbox="514 625 735 649">Artificial Intelligence</div> <div data-bbox="514 657 924 925"> <hr/> <p>Qualcomm® Adreno™ GPU</p> <hr/> <p>Qualcomm® Kryo™ CPU</p> <hr/> <p>Qualcomm® Hexagon™ Processor</p> <ul style="list-style-type: none"> • Fused AI Accelerator <ul style="list-style-type: none"> • Hexagon Tensor Accelerator • Hexagon Vector eXTensions • Hexagon Scalar Accelerator • Support for mix precision (INT8+INT16) • Support for all precisions (INT8, INT16, FP16) <hr/> <p>Qualcomm® Sensing Hub</p> </div> <div data-bbox="514 950 756 974">5G Modem-RF System</div> <div data-bbox="514 982 924 1356"> <hr/> <p>Snapdragon® X65 5G Modem-RF System</p> <ul style="list-style-type: none"> • 5G mmWave and sub-6 GHz, standalone • (SA) and non-standalone (NSA) modes, FDD, TDD • Dynamic Spectrum Sharing • mmWave: 8 carriers, 2x2 MIMO • Sub-6 GHz: 4x4 MIMO • Qualcomm® 5G PowerSave 2.0 • Qualcomm® Smart Transmit™ 2.0 technology • Qualcomm® Wideband Envelope Tracking • Qualcomm® AI-Enhanced Signal Boost • Global 5G multi-SIM <hr/> <p>Downlink: Up to 10 Gbps</p> <hr/> <p>Multimode support: 5G NR, LTE including CBRS, WCDMA, HSPA, CDMA 1x, EV-DO, GSM/EDGE</p> </div> <div data-bbox="966 625 1060 649">Camera</div> <div data-bbox="966 657 1375 1372"> <hr/> <p>Qualcomm Spectra™ Image Signal Processor</p> <ul style="list-style-type: none"> • Triple 18-bit ISPs • Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP) • Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag • Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag • Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag • Up to 200 Megapixel Photo Capture <hr/> <p>Rec. 2020 color gamut photo and video capture</p> <hr/> <p>Up to 10-bit color depth photo and video capture</p> <hr/> <p>8K HDR Video Capture + 64 MP Photo Capture</p> <hr/> <p>10-bit HEIF™: HEIC photo capture, HEVC video capture</p> <hr/> <p>Video Capture Formats: HDR10+, HDR10, HLG, Dolby Vision</p> <hr/> <p>8K HDR Video Capture @ 30 FPS</p> <hr/> <p>4K Video Capture @ 120 FPS</p> <hr/> <p>Slow-mo video capture at 720p @ 960 FPS</p> <hr/> <p>Bokeh Engine for Video Capture</p> <hr/> <p>Video super resolution</p> <hr/> <p>Multi-frame Noise Reduction (MFNR)</p> <hr/> <p>Locally Motion Compensated Temporal Filtering</p> <hr/> <p>Multi-Frame and triple exposure staggered/digital overlap HDR dual-sensor support</p> <hr/> <p>AI-based face detection, auto-focus, and</p> </div> <div data-bbox="1417 625 1470 649">CPU</div> <div data-bbox="1417 657 1827 738"> <hr/> <p>Kryo CPU</p> <ul style="list-style-type: none"> • Up to 3.2 GHz, with Arm Cortex-X2 technology • 64-bit Architecture </div> <div data-bbox="1417 763 1606 787">Visual Subsystem</div> <div data-bbox="1417 795 1827 1096"> <hr/> <p>Adreno GPU</p> <ul style="list-style-type: none"> • Vulkan® 1.1 API support • HDR gaming (10-bit color depth, Rec. 2020 color gamut) • Physically Based Rendering • Volumetric Rendering • Adreno Frame Motion Engine • API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1 • Hardware-accelerated H.265 and VP9 decoder • HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision </div> <div data-bbox="1417 1120 1501 1144">Security</div> <div data-bbox="1417 1153 1827 1364"> <hr/> <p>Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU)</p> <hr/> <p>Trust Management Engine</p> <hr/> <p>Qualcomm® wireless edge services (WES) and premium security features</p> <hr/> <p>Qualcomm® 3D Sonic Sensor and Qualcomm® 3D Sonic Max (fingerprint sensor)</p> <hr/> <p>Qualcomm® Type-1 Hypervisor</p> </div>

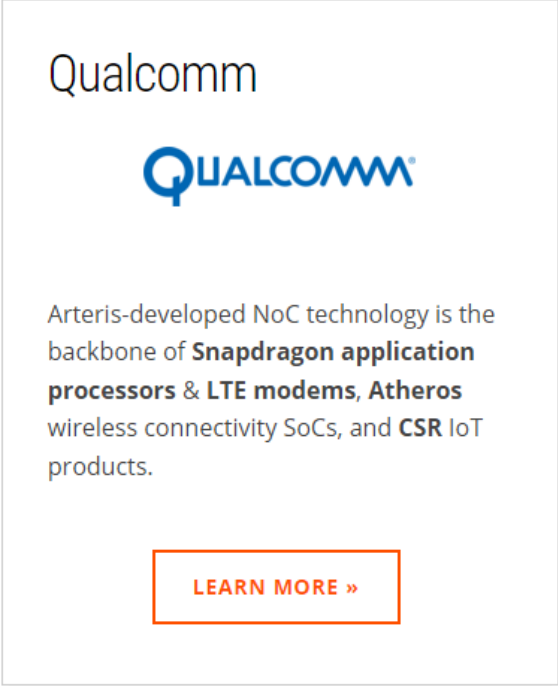
U.S. Patent No. 7,366,818 (Radulescu & Goossens)

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	OnePlus Product Including Snapdragon System on Chip ¹
	<p>Wi-Fi & Bluetooth*</p> <p>Qualcomm® FastConnect™ 6900 System</p> <ul style="list-style-type: none"> • Wi-Fi Standards: Wi-Fi 6E, Wi-Fi 6 (802.11ax), • Wi-Fi 5 (802.11ac), 802.11a/b/g/n • Wi-Fi Spectral Bands: 2.4 GHz, 5 GHz, 6 GHz • Peak speed: 3.6 Gbps • Channel Bandwidth: 20/40/80/160 MHz • 8-stream sounding (for 8x8 MU-MIMO) • MIMO Configuration: 2x2 (2-stream) • MU-MIMO (Uplink & Downlink) • 4K QAM • OFDMA (Uplink & Downlink) • 4-Stream (2x2 + 2x2) Dual Band Simultaneous (DBS) • Wi-Fi Security: WPA3-Enterprise, WPA3- Enhanced Open, WPA3 Easy Connect, WPA3-Personal <p>Integrated Bluetooth</p> <ul style="list-style-type: none"> • Bluetooth Features: Bluetooth® 5.3, LE Audio, Dual Bluetooth antennas • Bluetooth audio: Snapdragon Sound™ Technology with support for Qualcomm® aptX™ Voice, aptX Lossless, aptX Adaptive, and LE audio <p>snapdragon.com</p> <p><small>*Snapdragon 8+ Gen1 Mobile Platform also available in 3 GHz CPU version. Maximum CPU speed will vary based on platform version. Consult OEM specifications for device CPU speed. Certain optional features available subject to Carrier and OEM selection for an additional fee.</small></p> <p><small>Snapdragon, Qualcomm, Qualcomm Hexagon, Qualcomm 5G PowerSave, Qualcomm Kyro, Qualcomm Smart Transmit, Qualcomm Wideband Envelope Tracking, Qualcomm AI-Enhanced Signal Boost, Qualcomm Spectra, Qualcomm Agste, Qualcomm 3D Sonic Sensor, Qualcomm Type-T Hypervisor, Qualcomm Adreno, Qualcomm Sensing Hub, Qualcomm 3D Sonic Max, Qualcomm FastConnect, Snapdragon Sound, Qualcomm aptX, Snapdragon Elite Gaming, and Qualcomm Quick Charge are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm wireless edge services are offered by Qualcomm Technologies Inc. and/or its subsidiaries.</small></p> <p><small>Snapdragon, Qualcomm, Hexagon, Snapdragon Elite Gaming, Adreno, FastConnect, Snapdragon Sound, Kyro, Smart Transmit, Qualcomm Spectra, Qualcomm Agste, Snapdragon Sight, and Quick Charge are trademarks or registered trademarks of Qualcomm Incorporated. aptX is a trademark or registered trademark of Qualcomm Technologies International, Ltd.</small></p> <p><small>©2022 Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved.</small></p> <p>https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/Snapdragon-8-plus-Gen-1-Product-Brief.pdf</p>
a network (N; RN) arranged for	Without conceding that the preamble of claim 1 of the '818 Patent is limiting, the Snapdragon SoC included in the OnePlus product utilizes Arteris network on chip interconnect technology, and/or

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<p>providing at least one connection between a first and at least one second module (M, S), wherein said modules communicate via a network on chip, and</p>	<p>a derivative thereof, (collectively, the “Arteris NoC”) as a network (N; RN) arranged for providing connections between a first and at least one second module (M, S) in the Snapdragon SoC included in the OnePlus product, wherein said modules communicate via a network on chip, either literally or under the doctrine of equivalents.</p> <div data-bbox="512 456 1066 1138">  <p>Qualcomm</p> <p>Arteris-developed NoC technology is the backbone of Snapdragon application processors & LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products.</p> <p>LEARN MORE »</p> </div> <p>https://web.archive.org/web/20210514110614/https://www.arteris.com/customers</p>

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	<p data-bbox="575 293 1360 337">Certain Arteris Technology Assets Acquired</p> <p data-bbox="785 370 1150 394">by Kurt Shuler, on October 31, 2013</p> <p data-bbox="512 435 1255 459">Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP</p> <p data-bbox="512 483 1417 589">SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. (“Qualcomm”), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris.</p> <p data-bbox="512 621 1360 768">“Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris’ Network-on-Chip interconnect IP technology.</p> <p data-bbox="1234 816 1377 841">ARTERIS IP</p> <p data-bbox="1119 889 1377 906"><i>K. Charles Janoc, President and CEO, Arteris</i></p> <p data-bbox="499 971 1797 1044">https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team</p> <p data-bbox="499 1092 1843 1166">For example, in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p>

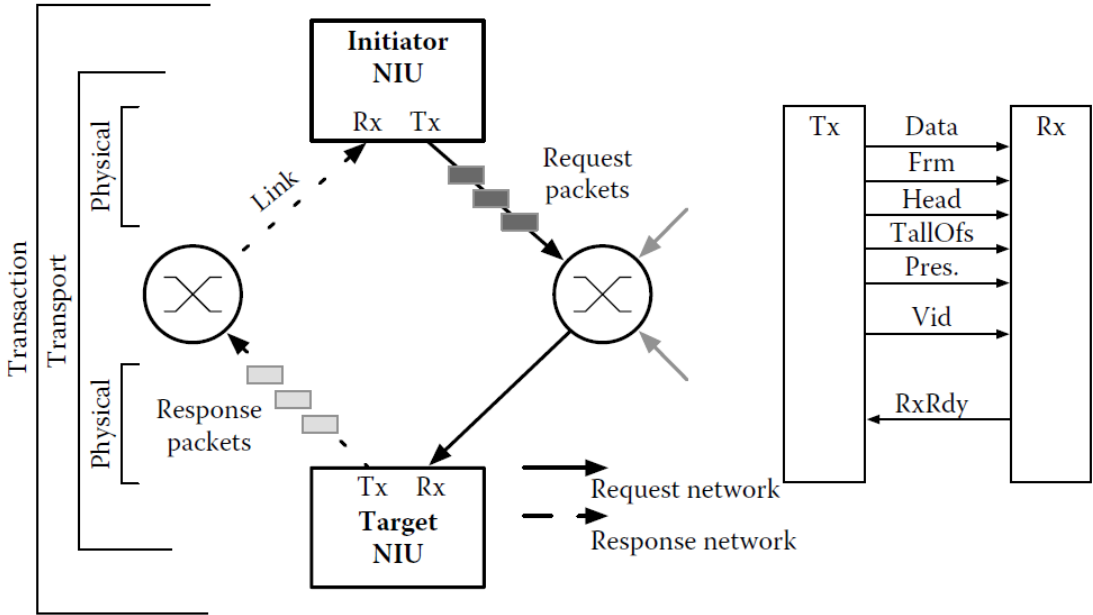
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	<p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p> <p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU’s Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: “In this chapter we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.”).</p> <p>A large SoC, such as the Snapdragon SoC included in the OnePlus product may include multiple classes of Arteris NoC:</p>

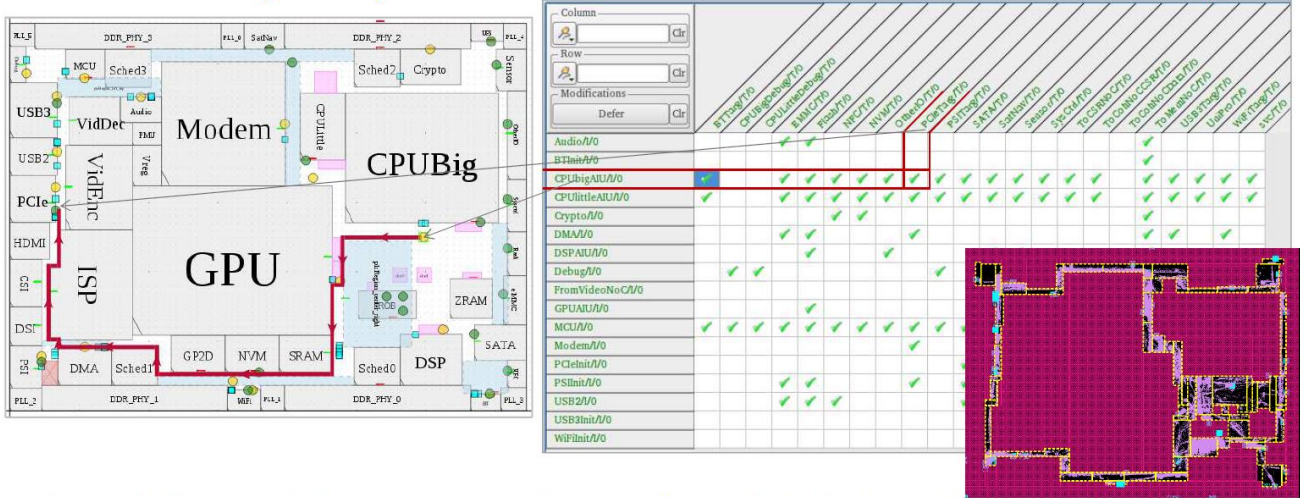

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	<div data-bbox="525 300 1575 357" style="text-align: center;"> <h2 style="color: orange;">Logical Interconnect Topology Development</h2> </div> <div data-bbox="525 365 1407 397" style="text-align: center;"> <p>FLEXNOC & NCORE INTERCONNECT IPS DEFINE ARCHITECTURES</p> </div> <div data-bbox="525 406 1092 828"> <p>The diagram illustrates a complex interconnect topology. At the top, various IP blocks are listed: CPU big, CPU lite, GPU, DSP, MMU, and others. These are connected to a central 'Main Interconnect' block. To the left, a 'Cache Coherent Interconnect' is shown, and below it, a 'Memory NoC' is depicted. The diagram uses color-coded lines to represent different types of connections and data flows.</p> </div> <div data-bbox="1092 406 1491 763"> <p>Two detailed network topology diagrams are shown. The top one is labeled 'Ncore Cache Coherent NoC' and the bottom one is 'Memory NoC'. Both show a grid-like structure with various nodes and connections, representing the internal network architecture of the system.</p> </div> <div data-bbox="1491 373 1869 844"> <p>Three more network topology diagrams are shown on the right side. The top one is 'Main NoC', the middle one is 'Service NoC', and the bottom one is 'Video NoC'. Each diagram shows a different network configuration, likely for different parts of the system or for different types of data traffic.</p> </div> <div data-bbox="525 844 1743 958"> <ul style="list-style-type: none"> • ArChip16 Example: Large SoCs have multiple classes of interconnect <ul style="list-style-type: none"> – Non-coherent, Coherent, Control/Status, Observability, etc. • Ncore & FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility </div> <div data-bbox="499 974 1879 1039" style="background-color: #f0f0f0; padding: 5px;"> <div style="display: flex; justify-content: space-between;"> ARTERIS IP ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 9 </div> </div> <div data-bbox="489 1076 1894 1149" data-label="Text"> <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.</p> </div> <div data-bbox="489 1193 1894 1273" data-label="Text"> <p>As a further illustration, connections between modules within the Arteris NoC may be defined by a connectivity table:</p> </div>

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	<p style="text-align: center; color: orange; font-weight: bold;">Connectivity Map → Interconnect Connections → Layout</p>  <ul style="list-style-type: none"> • Connectivity table defines interconnect connections within the floorplan • Routes must pass through available channels in the floorplan • Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU <p style="text-align: right;">DC-Topographical</p> <p style="text-align: center;">  ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 12 </p> <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.</p>
wherein said connection supports transactions comprising outgoing messages	<p>The Arteris NoC utilized by the Snapdragon SoC included in the OnePlus product has a connection that supports transactions comprising outgoing messages from the first module to the second modules and return messages from the second modules to the first module, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p>

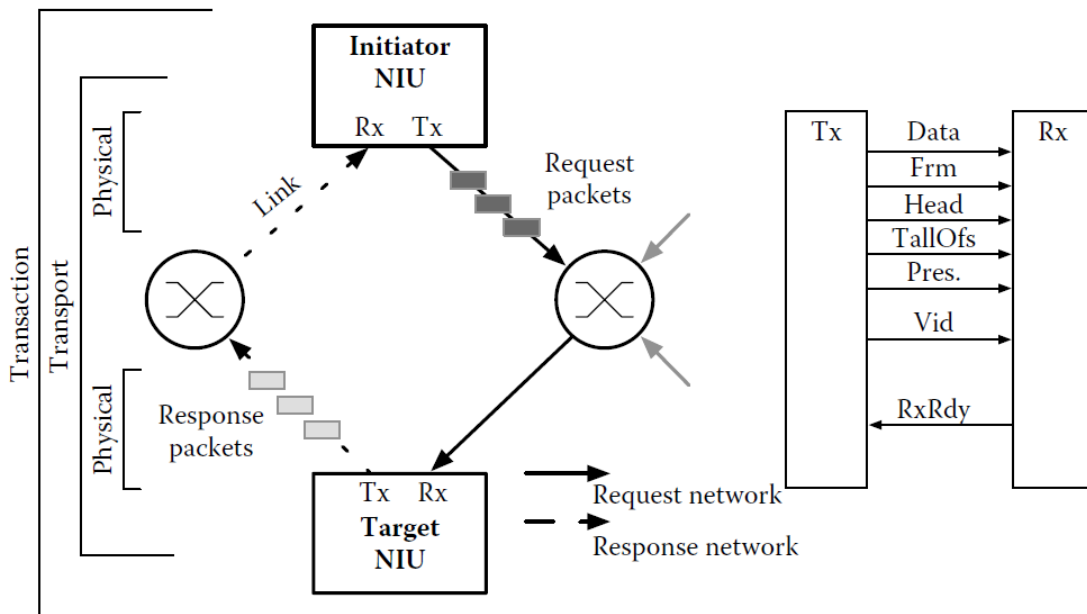
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from the first module to the second modules and return messages from the second modules to the first module	<p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p> <p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p>
the integrated circuit comprising at least one dropping means (DM) for dropping	The Arteris NoC utilized by the Snapdragon SoC included in the OnePlus product has at least one dropping means (DM) for dropping data exchanged by said first and second module (M, S), either literally or under the doctrine of equivalents.

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data exchanged by said first and second module (M, S), and

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For example, the Arteris NoC addresses packet corruption using, among other mechanisms, “packet validity checker” and “initiator timeout,” which may result in data being dropped:

Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; Initiator timeout
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

Functions

Failure Modes

Safety Mechanisms

10

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Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP,

https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation,

at 10.

As a further example, the Arteris NoC includes “packet validity checking” and “transaction timeout” for error resiliency, which may result in data being dropped:

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	<p><i>A. Advanced Data Protection and Reliability for SoC Interconnects</i></p> <p>Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller.</p> <p>The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent.</p> <p>Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf at 7.</p> <p>As a further example, in the Arteris NoC, “[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC,” which may result in data being dropped:</p>

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	<p><i>C. Transaction Timeout</i></p> <p>Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption.</p> <p>SoC Reliability Features in the FlexNoC Resilience Package, http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf at 2.</p>
<p>at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN),</p>	<p>The Arteris NoC utilized by the Snapdragon SoC included in the OnePlus product has at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN), either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p>

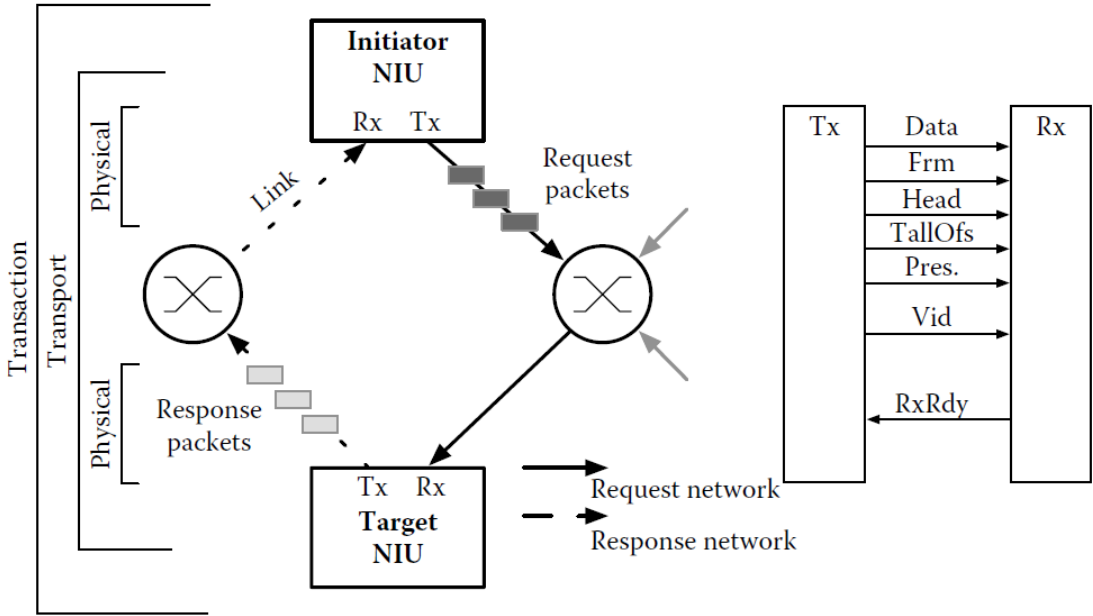
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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC,” and the Target NIUs are “used to connect a slave node to the NoC”:</p>

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“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	OnePlus Product Including Snapdragon System on Chip ¹
	<p data-bbox="520 305 1094 345">11.3.2 Network Interface Units</p> <p data-bbox="520 375 1856 513">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 553 1808 743" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="504 776 1808 849">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="504 894 1835 967">In the Arteris NoC “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC”:</p>

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	<p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

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	<p>burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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	<p style="text-align: center;">NIU Architecture</p> <p>The diagram illustrates the NIU Architecture, which is divided into two main sections: the Request Path and the Response Path. Both paths interface with an AHB Slave Interface on the left. The Request Path starts with an AHB Req (thick arrow) entering the AHB Slave Interface. Data flows from the AHB Slave Interface into a DATA FIFO, then to a Packet Assembly block, and finally to a PIPE bw/lw block, which connects to the Tx Port (thick arrow). The Response Path starts with an AHB Resp (thick arrow) entering the AHB Slave Interface. Data flows from the Rx Port (thick arrow) into a WIDTH CONVERTER (dashed box), then to a PIPE block, and finally to a FLOW CONTROL block. The FLOW CONTROL block sends information back to the AHB Slave Interface. Additionally, there is a CONTROL signal line connecting the FLOW CONTROL block to the Packet Assembly block. A TRANSLATION TABLE block is also present, receiving 'Add' and 'Ctrl' signals from a PIPE block and sending data to the BUILD HEADER & NECKER block, which then feeds into the Packet Assembly block.</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p> <p>As further example, “Target NIU units enable connection of a slave IP to the NoC by translating</p>

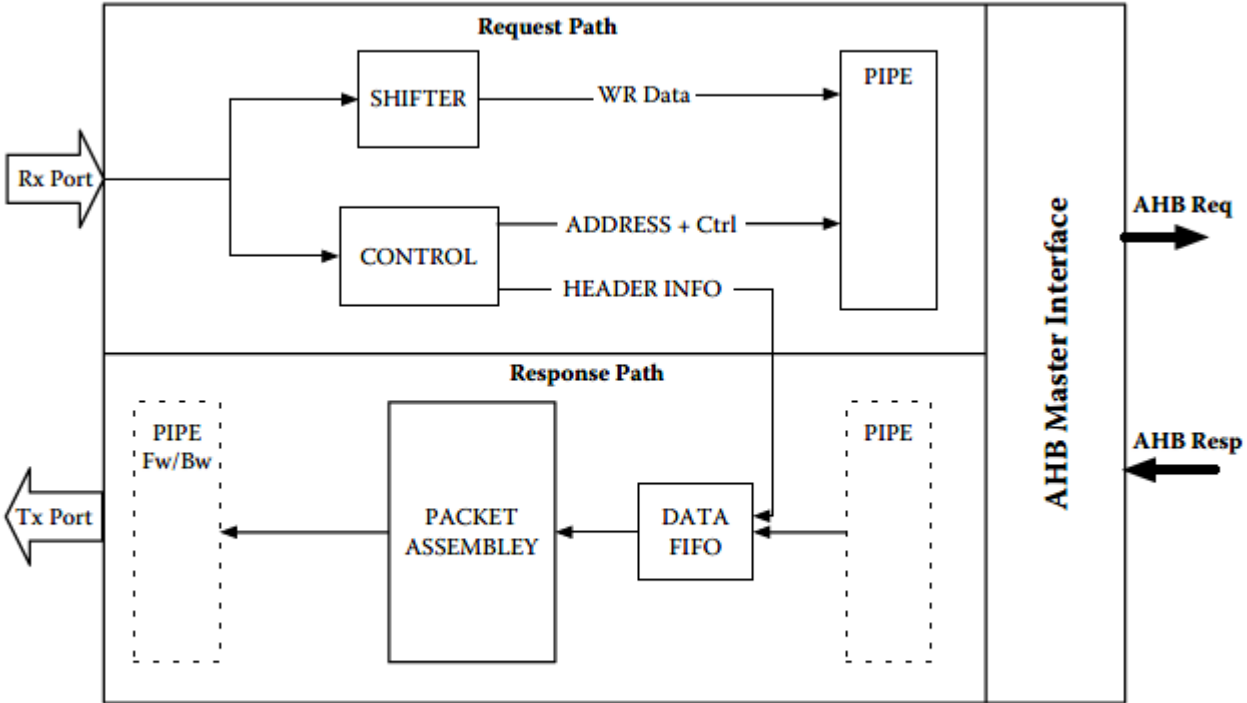
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	<p>NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets”:</p> <p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.</p>

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	<p style="text-align: center;">Target NIU Architecture</p>  <p>The diagram illustrates the Target NIU Architecture. It is divided into two main horizontal sections: the Request Path (top) and the Response Path (bottom). On the left, there is an Rx Port (input) and a Tx Port (output). The Request Path contains a SHIFTER block that receives data from the Rx Port and outputs WR Data to a PIPE block. A CONTROL block also receives data from the Rx Port and outputs ADDRESS + Ctrl and HEADER INFO to the same PIPE block. The Response Path contains a PACKET ASSEMBLY block that receives data from the Tx Port and outputs to a DATA FIFO block. The DATA FIFO block outputs to another PIPE block. The HEADER INFO from the Request Path is also fed into the DATA FIFO block. On the right, an AHB Master Interface block connects the internal architecture to the AHB bus, with AHB Req (request) and AHB Resp (response) signals.</p> <p>FIGURE 11.5 Network interface unit: Target architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.</p>

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<p>wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data, and</p>	<p>The interface means of the Arteris NoC utilized by the Snapdragon SoC included in the OnePlus product comprises a first dropping means (DM) for dropping data, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are “used to connect a master node to the NoC,” and the Target NIUs, that are “used to connect a slave node to the NoC”:</p> <p>11.3.2 Network Interface Units</p> <p>The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p>For example, the Arteris NoC addresses packet corruption using, among other mechanisms, “packet validity checker” and “initiator timeout,” which may result in data being dropped:</p>

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Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; Initiator timeout
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

Functions

Failure Modes

Safety Mechanisms

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Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP,

<https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation>, at 10.

As a further example, the Arteris NoC “can pass IP-generated error-correcting code (ECC) information through the NoC between the socket interfaces” and includes “packet validity checking” and “transaction timeout” for error resiliency, which may result in data being dropped:

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	<p><i>A. Advanced Data Protection and Reliability for SoC Interconnects</i></p> <p>Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller.</p> <p>The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent.</p> <p>Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf at 7.</p> <p>As a further example, in the Arteris NoC, “[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC,” which may result in data being dropped:</p>

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	<p><i>C. Transaction Timeout</i></p> <p>Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption.</p> <p>SoC Reliability Features in the FlexNoC Resilience Package, http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf at 2.</p>
<p>wherein the dropping of data and therefore the transaction completion can be controlled by the interface means.</p>	<p>In the Arteris NoC utilized by the Snapdragon SoC included in the OnePlus product, the transaction completion can be controlled by the interface means, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are “used to connect a master node to the NoC,” and the Target NIUs, that are “used to connect a slave node to the NoC”:</p> <p>11.3.2 Network Interface Units</p> <p>The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p>

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Functions

Failure Modes

Safety Mechanisms

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Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP,
<https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation>, at 10.

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